

1/3

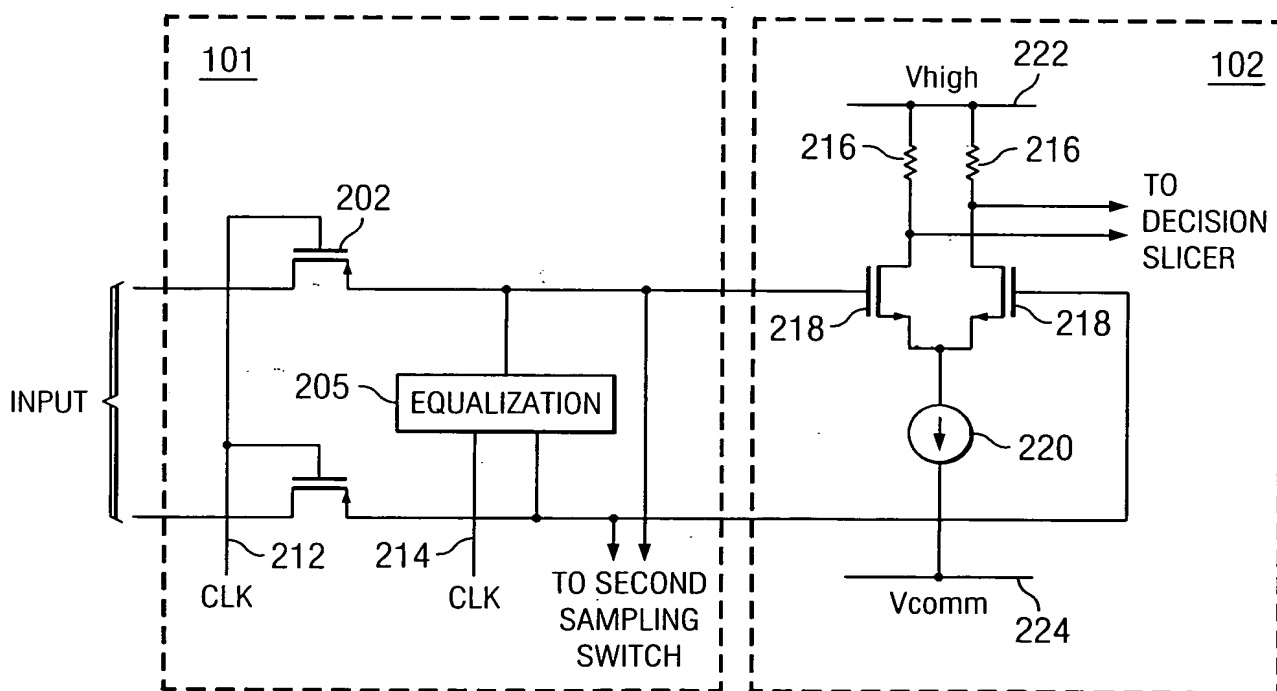
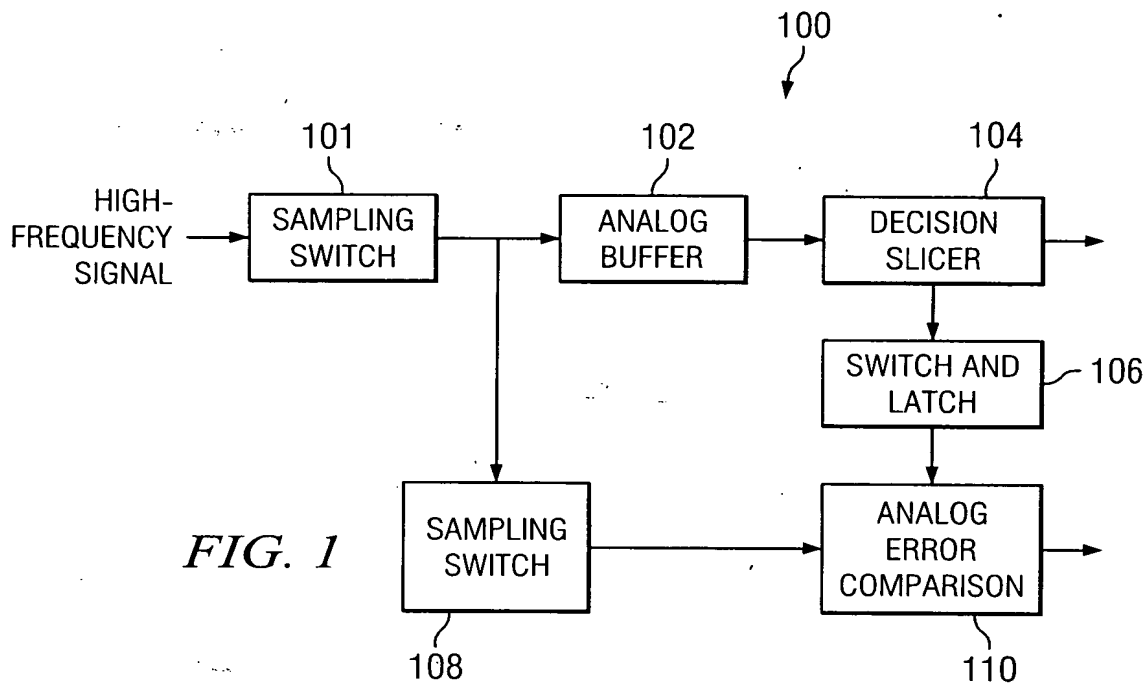


FIG. 3 is a schematic diagram of a circuit 104. The circuit includes a clock input CLK (302) and an input 'in'. The circuit is composed of several stages of transistors (304) and a feedback loop (306). The output of the circuit is labeled 104.

[illegible]

3/3

FIG. 5

